This listing of claims replaces all prior versions, and listings of claims in the instant application:

Listing of Claims:

1. (Original) A method of determining clock insertion delays for a microprocessor design having grid-based clock distribution, the method comprising:

partitioning the complete clock net into a global clock net and a plurality of local clock nets;

simulating each of the plurality of local clock nets to generate a load for each of the plurality of local clock nets on the global clock net;

simulating the global clock net based in part on the simulated load of each of the plurality of local clock nets;

combining the plurality of simulations to form the complete clock net;

storing the plurality of simulation results in a Clock Data Model; and

evaluating the plurality of simulation results to determine whether the results converge.

2. (Original) The method as defined in claim 1, wherein partitioning comprises breaking the complete clock net into equal sized parts according to rectangular grid coordinates.

3. (Original) The method as defined in claim 1, further comprising breaking at least one of the plurality of local clock nets down into at least one sub-local clock net.

4. (Original) The method as defined in claim 3, further comprising simulating the at least one sub-local clock net prior to simulating the corresponding local clock net.

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5. (Original) The method as defined in claim 1, wherein at least two of the plurality of local clock nets are simulated in parallel.

6. (Original) The method as defined in claim 1, wherein simulating each of the plurality of local clock nets comprises:

extracting a layout of the local clock net and the conductors routed above and through the local clock net from a microprocessor network database;

extracting component values of the elements of the local clock net from the microprocessor network database;

simulating the local clock net based on the layout and the component values; and

extracting a load of the local clock net on the global clock net.

7. (Original) The method as defined in claim 6, wherein simulating the local clock net comprises assuming that the clock arrival times from the global clock net will be simultaneous at all points where the local clock net is connected to the global clock net.

8. (Original) The method as defined in claim 1, wherein simulating the global clock net comprises:

extracting the layout of the global clock net from a microprocessor network database;

extracting component values of the elements of the global clock net from the microprocessor network database;

inserting the simulated loads of the plurality of local clock nets; and

simulating the global clock net based on the layout, the component values, and the simulated local clock net loads.

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9. (Original) The method as defined in claim 1, wherein, if the results do not converge, the method further comprises:

assuming that clock arrival times are those calculated for the simulated global clock net;

re-simulating at least one of the plurality of local clock nets to generate a load for the at least one local clock net on the global clock net;

re-simulating the global clock net based in part on the simulated or re-simulated load of each of the plurality of local clock nets; and

combining the simulations and re-simulations to form the complete clock net.

10. (Original) The method as defined in claim 9, wherein re-simulating at least one of the plurality of local clock nets comprises:

re-simulating the at least one local clock net based on the layout, the component values, and the calculated clock arrival times; and

extracting a load of the at least one local clock net on the global clock net.

11. (Original) The method as defined in claim 10, further comprising re-simulating at least a second of the plurality of local clock nets in parallel with the at least one local clock net.

12. (Original) The method as defined in claim 9, wherein re-simulating the global clock net comprises:

inserting the simulated or re-simulated loads of the plurality of local clock nets; and

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re-simulating the global clock net based on the layout, the component values, and the simulated or re-simulated local clock net loads.

13. (Original) The method as defined in claim 9, further comprising storing the plurality of re-simulation results in the Clock Data Model.

14. (Original) An apparatus for determining clock insertion delays for a microprocessor design having grid-based clock distribution, the apparatus comprising:

means for partitioning the complete clock net into a global clock net and a plurality of local clock nets;

means for simulating each of the plurality of local clock nets to generate a load for each of the plurality of local clock nets on the global clock net;

means for simulating the global clock net based in part on the simulated load of each of the plurality of local clock nets;

means for combining the plurality of simulations to form the complete clock net;

means for storing the plurality of simulation results in a Clock Data Model; and

means for evaluating the plurality of simulation results to determine whether the results converge.

15. (Original) The apparatus as defined in claim 14, wherein means for partitioning comprises means for breaking the complete clock net into equal sized parts according to rectangular grid coordinates.

16. (Original) The apparatus as defined in claim 14, further comprising means for breaking at least one of the

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plurality of local clock nets down into at least one sub-local clock net.

17. (Original) The apparatus as defined in claim 16, further comprising means for simulating the at least one sub-local clock net prior to simulating the corresponding local clock net.

18. (Original) The apparatus as defined in claim 14, wherein at least two of the plurality of local clock nets are simulated in parallel.

19. (Original) The apparatus as defined in claim 14, wherein means for simulating each of the plurality of local clock nets comprises:

means for extracting a layout of the local clock net and the conductors routed above and through the local clock net from a microprocessor network database;

means for extracting component values of the elements of the local clock net from the microprocessor network database;

means for simulating the local clock net based on the layout and the component values; and

means for extracting a load of the local clock net on the global clock net.

20. (Original) The apparatus as defined in claim 19, wherein means for simulating the local clock net comprises means for assuming that the clock arrival times from the global clock net will be simultaneous at all points where the local clock net is connected to the global clock net.

21. (Original) The apparatus as defined in claim 14, wherein means for simulating the global clock net comprises:

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means for extracting the layout of the global clock net from a microprocessor network database;

means for extracting component values of the elements of the global clock net from the microprocessor network database;

means for inserting the simulated loads of the plurality of local clock nets; and

means for simulating the global clock net based on the layout, the component values, and the simulated local clock net loads.

22. (Original) The apparatus as defined in claim 14, wherein the apparatus further comprises:

means for assuming that clock arrival times are those calculated for the simulated global clock net;

means for re-simulating at least one of the plurality of local clock nets to generate a load for the at least one local clock net on the global clock net;

means for re-simulating the global clock net based in part on the simulated or re-simulated load of each of the plurality of local clock nets; and

means for combining the simulations and re-simulations to form the complete clock net.

23. (Original) The apparatus as defined in claim 22, wherein means for re-simulating at least one of the plurality of local clock nets comprises:

means for re-simulating the at least one local clock net based on the layout, the component values, and the calculated clock arrival times; and

means for extracting a load of the at least one local clock net on the global clock net.

24. (Original) The apparatus as defined in claim 23, further comprising means for re-simulating at least a second of

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the plurality of local clock nets in parallel with the at least one local clock net.

25. (Original) The apparatus as defined in claim 22, wherein means for re-simulating the global clock net comprises:
means for inserting the simulated or re-simulated loads of the plurality of local clock nets; and
means for re-simulating the global clock net based on the layout, the component values, and the simulated or re-simulated local clock net loads.

26. (Original) The apparatus as defined in claim 22, wherein the re-simulation results are stored in the Clock Data Model.

27. (Currently Amended) An apparatus for determining clock insertion delays for a microprocessor design having grid-based clock distribution, the apparatus comprising:
a partitioner for horizontally and vertically partitioning the complete clock net into a global clock net and a plurality of local clock nets, wherein;
the partitioner vertically sub-partitions at least one of the plurality of local clock nets down into at least one sub-local clock net;
at least one local clock net simulator for simulating at least one of the plurality of local clock nets to generate a load for the at least one local clock net on the global clock net, wherein;
the at least one local clock net simulator simulates the at least one sub-local clock net prior to simulating the corresponding local clock net;
a global clock net simulator for simulating the global clock net based in part on the simulated load of each of the plurality of local clock nets;

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a merging unit for combining the plurality of simulations to form the complete clock net;

a Clock Data Model for storing the plurality of simulation results; and

a convergence evaluator for evaluating the plurality of simulation results to determine whether the results converge.

28. (Original) The apparatus as defined in claim 27, wherein the partitioner comprises a cutter for breaking the complete clock net into equal sized parts according to rectangular grid coordinates.

29. (Cancelled) - Please Cancel Claim 29, without prejudice.

30. (Cancelled) - Please Cancel Claim 30, without prejudice.

31. (Original) The apparatus as defined in claim 27, further comprising at least a second local clock net simulator wherein at least a second of the plurality of local clock nets is simulated in parallel with the at least one local clock net.

32. (Original) The apparatus as defined in claim 27, wherein the at least one local clock net simulator comprises:

a layout extractor for extracting a layout of the local clock net and the conductors routed above and through the local clock net from a microprocessor network database;

a component value extractor for extracting component values of the elements of the local clock net from the microprocessor network database;

a local clock net simulator for simulating the local clock net based on the layout and the component values; and

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a load extractor for extracting a load of the local clock net on the global clock net.

33. (Currently Amended) The apparatus as defined in claim ~~36~~ 26, wherein the local clock net simulator assumes for the simulation that the clock arrival times from the global clock net will be simultaneous at all points where the local clock net is connected to the global clock net.

34. (Original) The apparatus as defined in claim 27, wherein the global clock net simulator comprises:

a layout extractor for extracting the layout of the global clock net from a microprocessor network database;

a component extractor for extracting component values of the elements of the global clock net from the microprocessor network database;

a load insertion unit for inserting the simulated loads of the plurality of local clock nets; and

a simulator for simulating the global clock net based on the layout, the component values, and the simulated local clock net loads.

35. (Original) The apparatus as defined in claim 27, wherein, when the results are found not to converge:

the apparatus assumes that clock arrival times are those calculated for the simulated global clock net;

the at least one local clock net simulator re-simulates at least one of the plurality of local clock nets to generate a load for the at least one local clock net on the global clock net;

the global clock net simulator re-simulates the global clock net based in part on the simulated or re-simulated load of each of the plurality of local clock nets; and

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the merging unit combines the simulations and re-simulations to form the complete clock net.

36. (Original) The apparatus as defined in claim 35, wherein the plurality of re-simulation results are stored in the Clock Data Model.

37. (Original) A computer-readable medium having stored thereon computer-executable instructions for performing a method of determining clock insertion delays for a microprocessor design having grid-based clock distribution, the method comprising:

partitioning the complete clock net into a global clock net and a plurality of local clock nets;

simulating each of the plurality of local clock nets to generate a load for each of the plurality of local clock nets on the global clock net;

simulating the global clock net based in part on the simulated load of each of the plurality of local clock nets;

combining the plurality of simulations to form the complete clock net;

storing the plurality of simulation results in a Clock Data Model; and

evaluating the plurality of simulation results to determine whether the results converge.

38. (Original) The computer-readable medium as defined in claim 37, wherein partitioning comprises breaking the complete clock net into equal sized parts according to rectangular grid coordinates.

39. (Original) The computer-readable medium as defined in claim 37, wherein the method further comprises breaking at

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least one of the plurality of local clock nets down into at least one sub-local clock net.

40. (Original) The computer-readable medium as defined in claim 39, wherein the method further comprises simulating the at least one sub-local clock net prior to simulating the corresponding local clock net.

41. (Original) The computer-readable medium as defined in claim 37, wherein at least two of the plurality of local clock nets are simulated in parallel.

42. (Original) The computer-readable medium as defined in claim 37, wherein simulating each of the plurality of local clock nets comprises:

extracting a layout of the local clock net and the conductors routed above and through the local clock net from a microprocessor network database;

extracting component values of the elements of the local clock net from the microprocessor network database;

simulating the local clock net based on the layout and the component values; and

extracting a load of the local clock net on the global clock net.

43. (Original) The computer-readable medium as defined in claim 42, wherein simulating the local clock net comprises assuming that the clock arrival times from the global clock net will be simultaneous at all points where the local clock net is connected to the global clock net.

44. (Original) The computer-readable medium as defined in claim 37, wherein simulating the global clock net comprises:

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extracting the layout of the global clock net from a microprocessor network database;

extracting component values of the elements of the global clock net from the microprocessor network database;

inserting the simulated loads of the plurality of local clock nets; and

simulating the global clock net based on the layout, the component values, and the simulated local clock net loads.

45. (Original) The computer-readable medium as defined in claim 37, wherein, if the results do not converge, the method further comprises:

assuming that clock arrival times are those calculated for the simulated global clock net;

re-simulating at least one of the plurality of local clock nets to generate a load for the at least one local clock net on the global clock net;

re-simulating the global clock net based in part on the simulated or re-simulated load of each of the plurality of local clock nets; and

combining the simulations and re-simulations to form the complete clock net.

46. (Original) The computer-readable medium as defined in claim 45, wherein re-simulating at least one of the plurality of local clock nets comprises:

re-simulating the at least one local clock net based on the layout, the component values, and the calculated clock arrival times; and

extracting a load of the at least one local clock net on the global clock net.

47. (Original) The computer-readable medium as defined in claim 46, wherein the method further comprises re-simulating

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patenting over Claims 1 to 77 of co-pending Application no. 09/982,452.

Applicants respectfully note that the Examiner's rejection is provisional and therefore dependent on the issuance of Claims 1 to 77 of co-pending Application no. 09/982,452. Consequently, Applicants elect to respond to the provisional rejection of Claims 1 to 49 under the judicially created doctrine of obviousness-type double patenting over Claims 1 to 77 of co-pending Application no. 09/982,452 upon issuance of any, or all, of Claims 1 to 77 of co-pending Application no. 09/982,452.

REJECTION OF CLAIMS 1 TO 49 UNDER 35 U.S.C. 103(a)

The Examiner rejected Claims 1 to 49 under 35 U.S.C. 103(a) as obvious over the Camporese et al. reference (US 6,205,571) in view of the Graef reference (US 6,305,001).

Applicants have cancelled Claims 29 and 30, without prejudice.

Applicants' independent Claim 1 recites, with emphasis added:

> A method of determining clock insertion delays for a microprocessor design having grid-based clock distribution, the method comprising:
>
> partitioning the complete clock net into a global clock net and a plurality of local clock nets;
>
> **simulating each of the plurality of local clock nets to generate a load for each of the plurality of local clock nets on the global clock net;**
>
> **simulating the global clock net based in part on the simulated load of each of the plurality of local clock nets;**
>
> **combining the plurality of simulations to form the complete clock net;**
>
> storing the plurality of simulation results in a Clock Data Model; and

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evaluating the plurality of simulation results to determine whether the results converge.

Applicants' independent Claim 14 recites, with emphasis added:

An apparatus for determining clock insertion delays for a microprocessor design having grid-based clock distribution, the apparatus comprising:
means for partitioning the complete clock net into a global clock net and a plurality of local clock nets;
means for **simulating each of the plurality of local clock nets to generate a load for each of the plurality of local clock nets on the global clock net;**
means for **simulating the global clock net based in part on the simulated load of each of the plurality of local clock nets;**
means for **combining the plurality of simulations to form the complete clock net;**
means for storing the plurality of simulation results in a Clock Data Model; and
means for evaluating the plurality of simulation results to determine whether the results converge.

Applicants' independent Claim 37 recites, with emphasis added:

A computer-readable medium having stored thereon computer-executable instructions for performing a method of determining clock insertion delays for a microprocessor design having grid-based clock distribution, the method comprising:
partitioning the complete clock net into a global clock net and a plurality of local clock nets;
simulating each of the plurality of local clock nets to generate a load for each of the plurality of local clock nets on the global clock net;

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at least a second of the plurality of local clock nets in parallel with the at least one local clock net.

48. (Original) The computer-readable medium as defined in claim 45, wherein re-simulating the global clock net comprises:

inserting the simulated or re-simulated loads of the plurality of local clock nets; and

re-simulating the global clock net based on the layout, the component values, and the simulated or re-simulated local clock net loads.

49. (Original) The computer-readable medium as defined in claim 45, wherein the method further comprises storing the plurality of re-simulation results in the Clock Data Model.

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